REMARKS

Applicant has attached hereto a copy of the certified English translation of the priority document corresponding to French patent application No. 0450324, filed on February 20, 2004. A copy of the certified priority document and a copy of the Declaration and Power of Attorney as filed, claiming priority to the above French application, are also attached.

In accordance with the MPEP § 201.14(a)(2) applicant is entitled to the priority date based upon claiming priority and submitting a copy of the certified priority document to the patent office before the patent issues. Applicants claim to priority is not determined by the PALM system as apparently alleged by the Examiner in paragraph 5 of page 3. Based upon the perfection of the claim to priority, the cited reference Risen, having a filing date of July 8, 2004 which is subsequent to the effective filing date of applicant of February 20, 2004, is antedated and should be withdrawn as a reference from the rejection of the claims.

In view of the above, all of the rejections of claims 1-59 under 35 USC 103(a) are based upon the cited reference Risen which is no longer applicable and accordingly should be withdrawn.

The rejection of claims 35-37 under 35 USC 102(b) as being anticipated by USP 6,606,707 to Hiruta et al is respectfully traversed.

Applicant has amended claim 35, 38 as well as 39 to clearly overcome the rejection of claims 35-37 as being anticipated under 35 USC 102(b).

Claim 35 now clearly calls for a plurality of removable security interfaces, and a plurality of reception equipment and a plurality of conditional access control cards to manage access to digital data distributed by an operator. Each of the plurality of removable interfaces include a non-volatile memory containing memorized information of unique identifiers for subscribers and means for verifying if the unique identifier in a control card is present in the list memorized in said non-volatile memory of a removable interface, none of which is taught in Hirota et al. Hirota et al does not even teach use of a plurality of security interfaces or a plurality of reception equipment and/or control cards. Accordingly, claim 35, as amended, is clearly patentable over Hirota et al under 35 USC 102(b).

Claims 36-37 depend from claim 35 and are therefore believed patentable for the same reason given above. Accordingly, the rejection of claims 35-37 under 35 USC 102(b) should be withdrawn.

Applicant has further amended claims 1, 10-14, 23-28 as well as claim 39 to place the application in condition for allowance, even if Risan were considered to be prior art. The applicant wishes to make it of record that neither Hirota nor Risan disclose or suggest a method for matching a number N of data reception equipment with a number M in a plurality of external security modules which comprise:

- a configuration phase remotely controlled by an operator and comprising the following steps:

- memorizing a list of identifiers of reception equipment in each external security module;

memorizing a list of identifiers of external security module in each reception equipment; and

- carrying out a check phase when an external security module is conenct3d to a reception equipment to control whether or not the identifiers of external security module is present in the list memorized in this reception equipment, and if the identifier of said reception equipment is present in the list memorized n said external security module, wherein, the operator transmits a signal to the reception equipment to manage a check phase comprising at least one of the following set values:

- activating the check phase at a programmed date or after a programmed delay,

- deactivating the check phase at a programmed date or after the programmed delay,

- specifying an absolute date (or a delay_ starting from which (or after which) the check phase is activated or deactivated and

- canceling said programmed date (or said programmed delay).

Hirota teaches a semiconductor memory card comprising an authentication area for storing copyright protected digital contents and a non-authentication area for storing other date and is not related to use of a plurality of reception equipment.

The semiconductor memory of Hirota further comprises an authentication unit to manage access to the authentication area. At Col. 5, lines 9-17, Hirota recites: "In the

above semiconductor memory card, the authentication unit may request a user of the electronic device to input a user key which is information unique to the user, during the authentication process, and the control circuit further includes: a user key storage unit which stores the user key; an identification information identifying an electronic device that has been affirmatively authenticated by the authentication unit".

At col. 5, lines 18-29, Hirota teaches that "after the authentication unit starts the authentication process, a prohibition unit which obtains a piece of identification information from a target electronic device checks whether the piece of identification information obtained from the target electronic has already been stored in the identification storage unit and prohibit the authentication unit from requesting a user of the electronic device to input a user key when the piece of identification information from a target electronic device has already been stored in the identification storage unit".

The check process described above prevents the user from entering a key in the authentication unit when the identification information of said user is already registered within the identification storage.

The process in Hitora has no relevance to check phase of claim 1 which is remotely controlled by the operator to determine whether or not identifiers of external security modules are present in a list memorized in a reception equipment and identifiers of said reception equipment are present in a list memorized in said external security modules in order to authorize or prevent access, by the reception equipment, to data distributed by the operator.

In Hirota, the authentication unit is used to determine whether or not an electronic device may access to a storage area in a semiconductor memory or not.

Accordingly, no basis exists to combine Risan with Hitora to realize matching a number N of data reception equipment with a number M of external security modules because none of these references disclose or suggest such matching.

For all of the above reasons, claims 1-59 are now clearly in condition for allowance.

Reconsideration and allowance of claims 1-59 is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence w/attachments is being transmitted to the USPTO via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450, on December 20, 2011 .

By _____